ĐẠI HỌC QUỐC GIA

ĐẠI HỌC BÁCH KHOA TP HỒ CHÍ MINH

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LSI Logic Design Report Lab 4

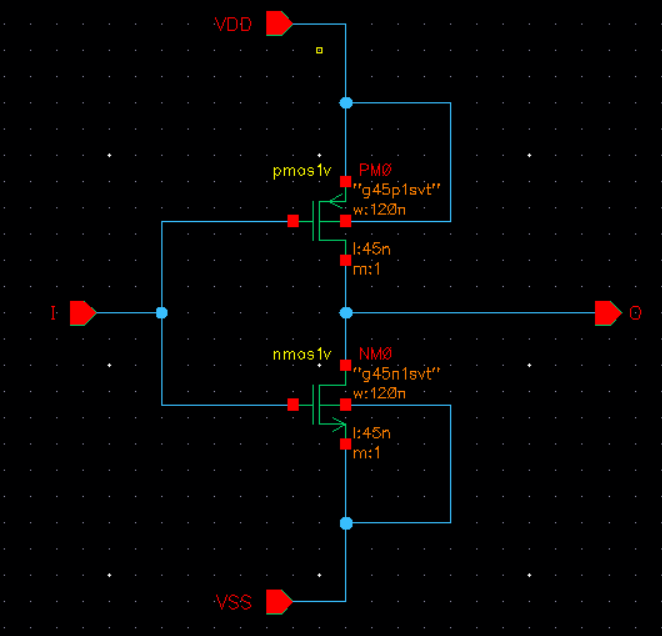
Instructor: Nguyễn Thiên Ân

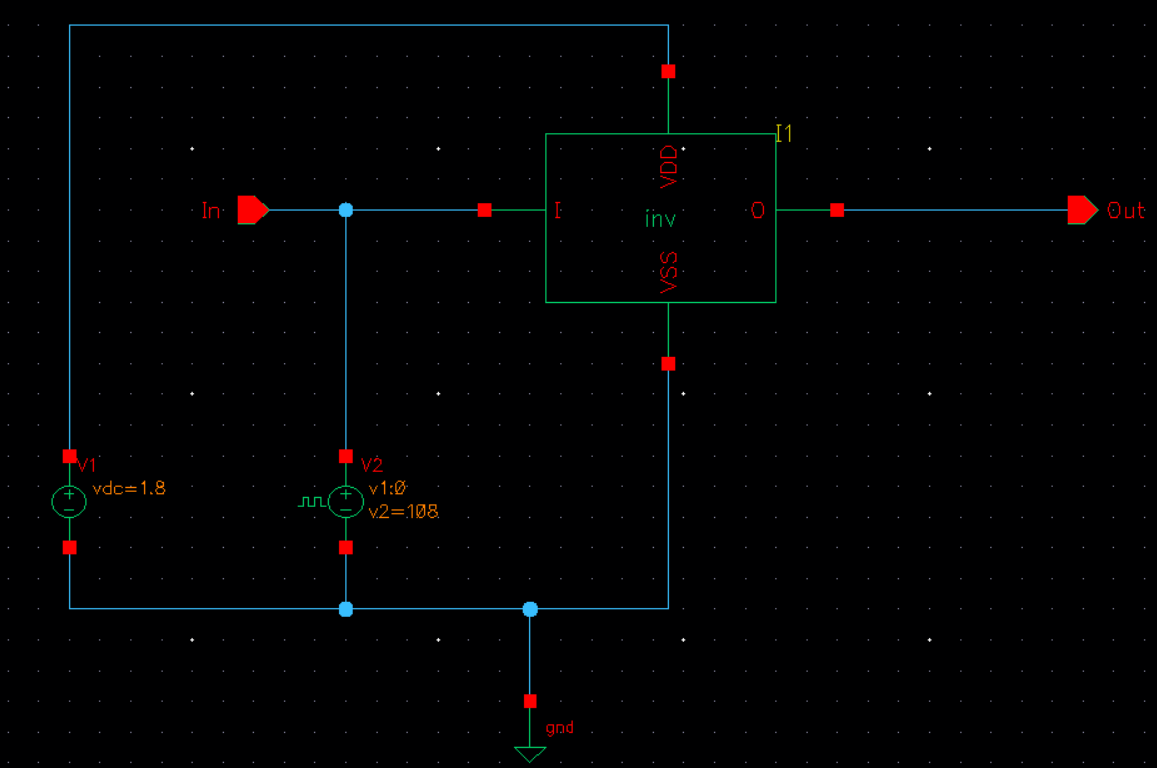
Student: Lê Gia Huy – Student ID: 1952717

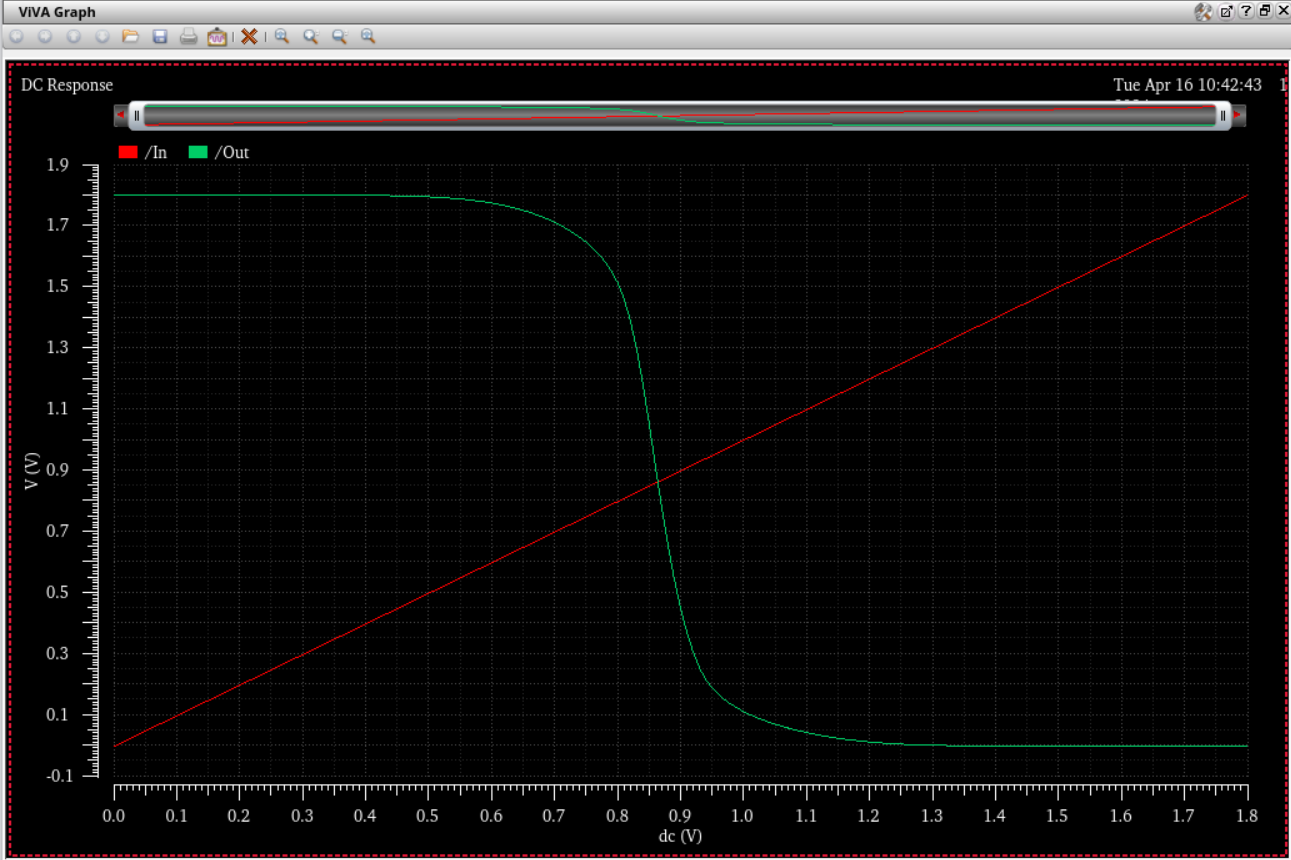
*Thành phố Hồ Chí Minh – 2024*

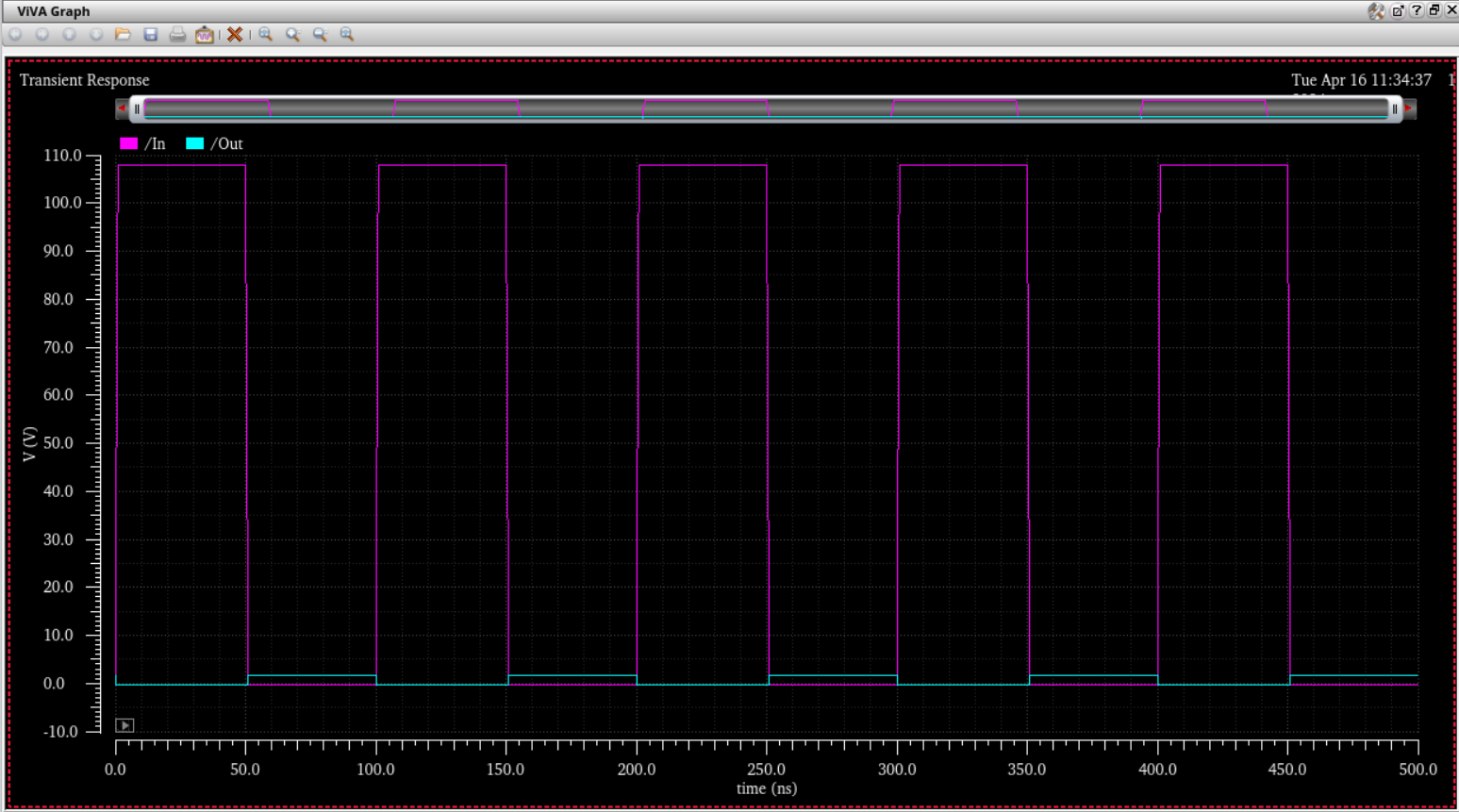
1. **INVERTE GATE**

**1. Schematic**

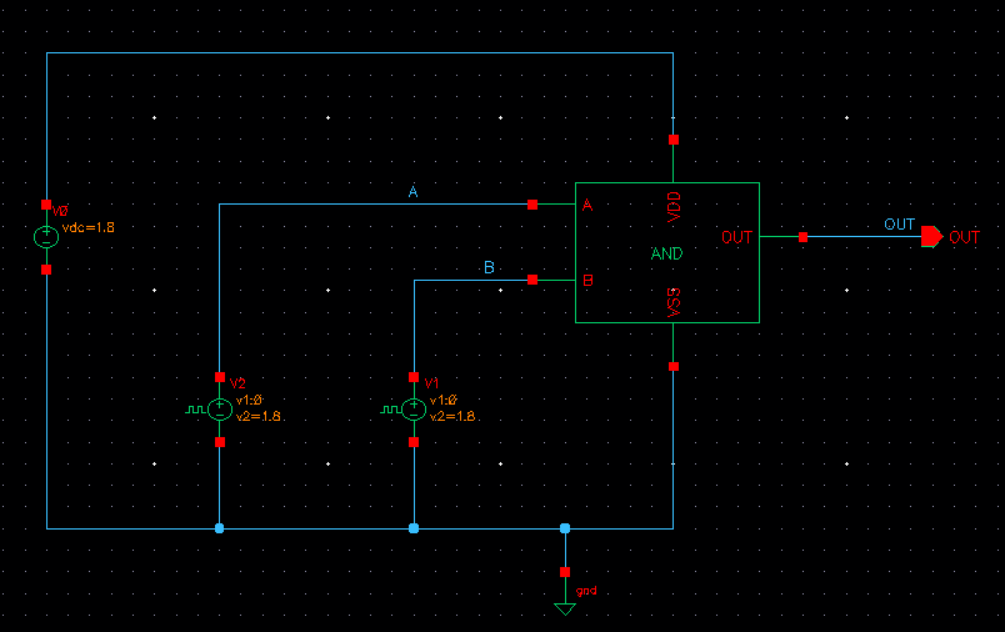
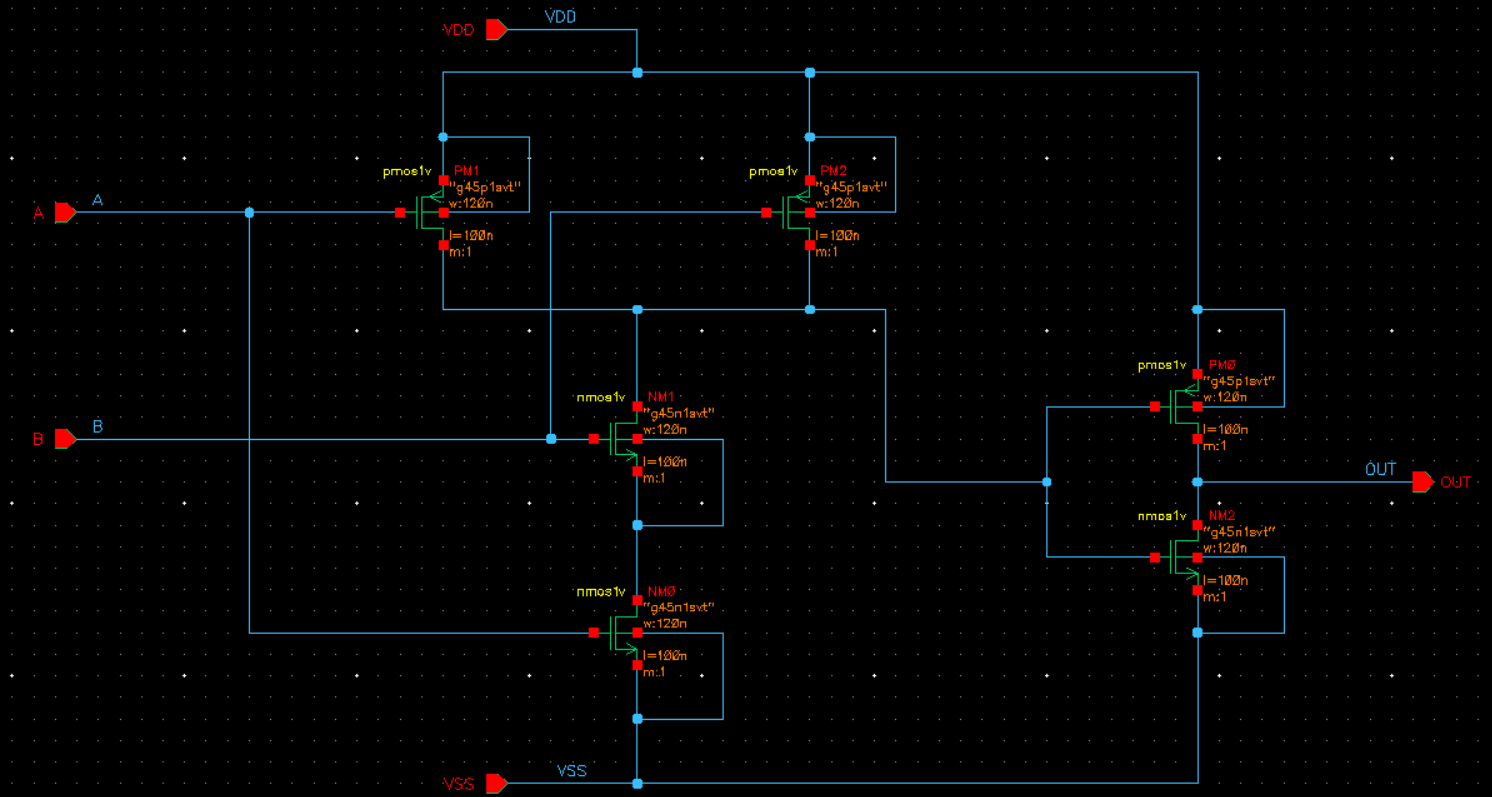
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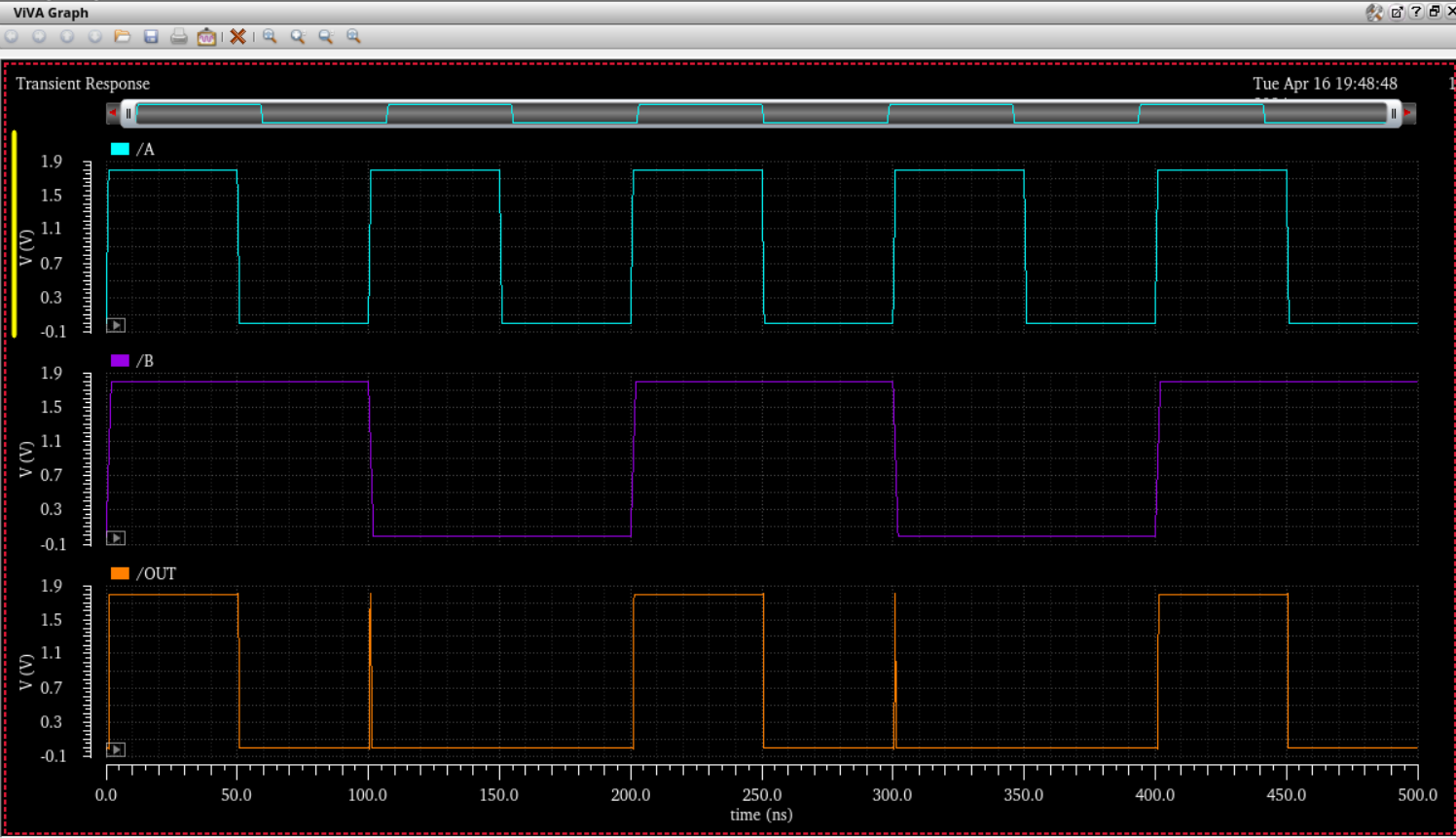


2. Simulation result

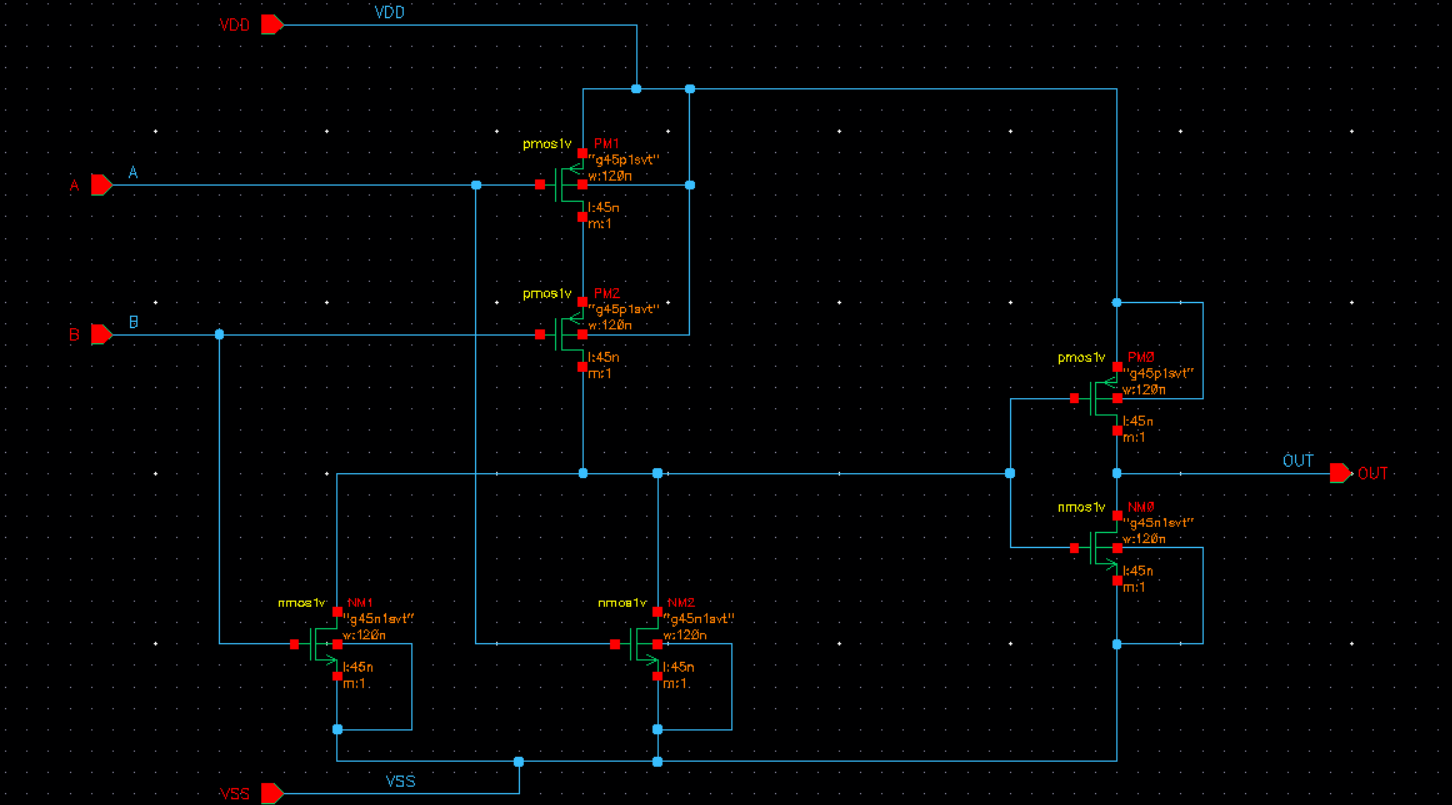


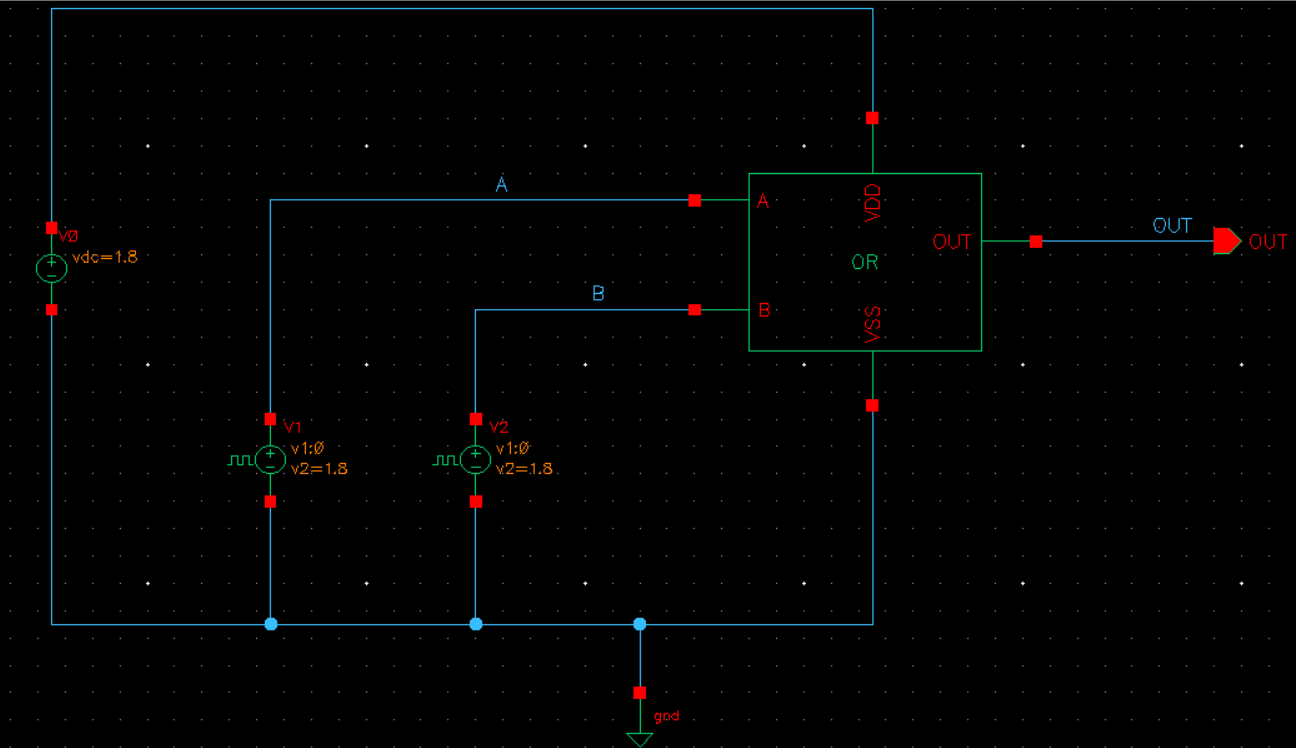
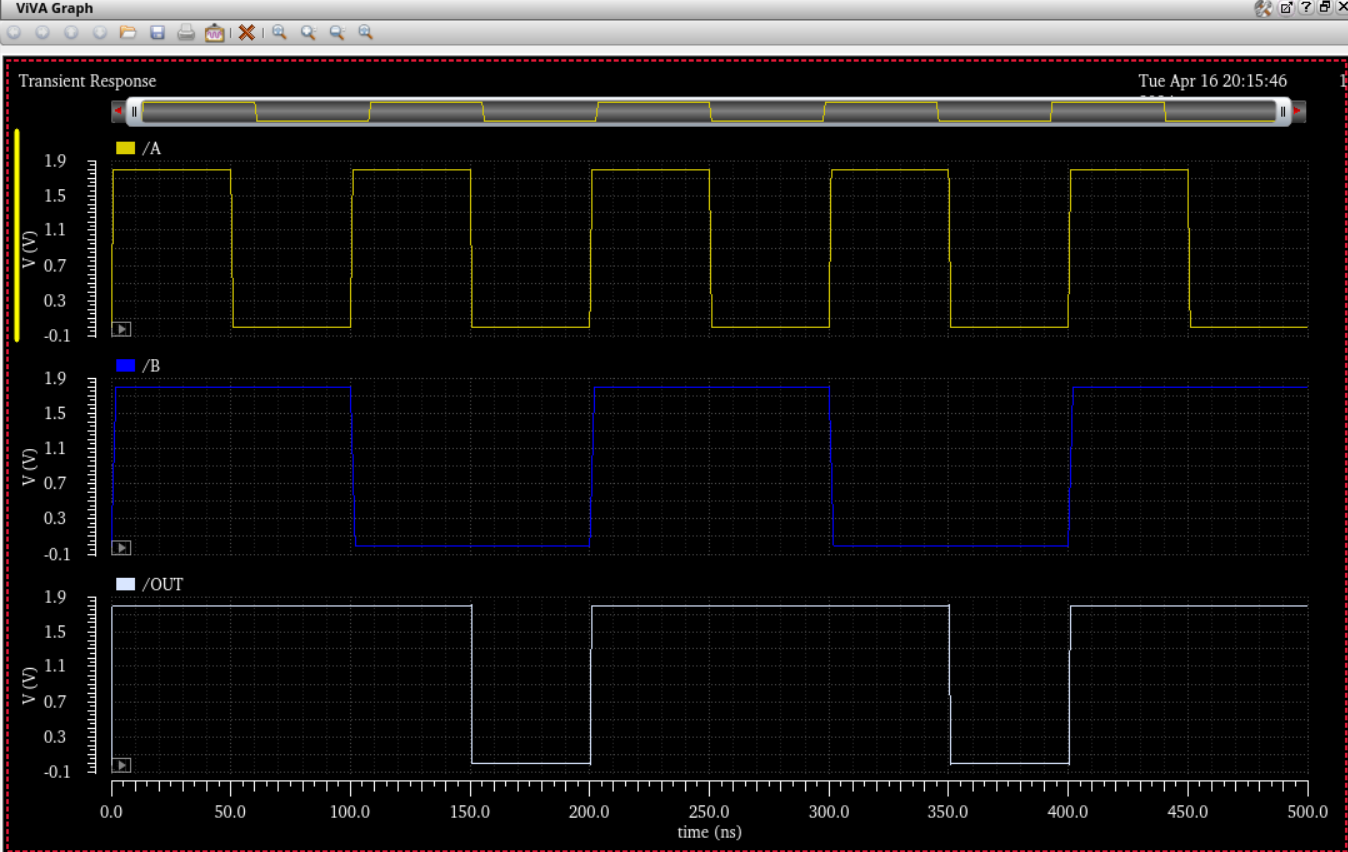
1. **AND GATE**

**1. Schemetic**

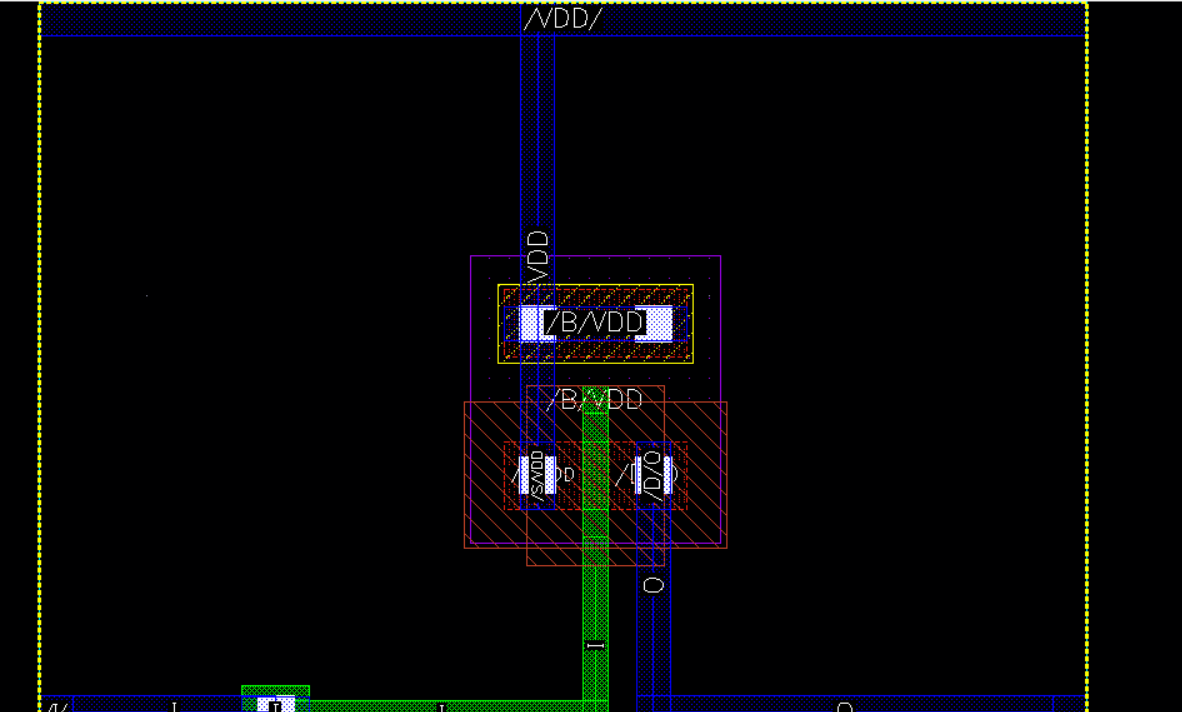
**2. Simulation results**

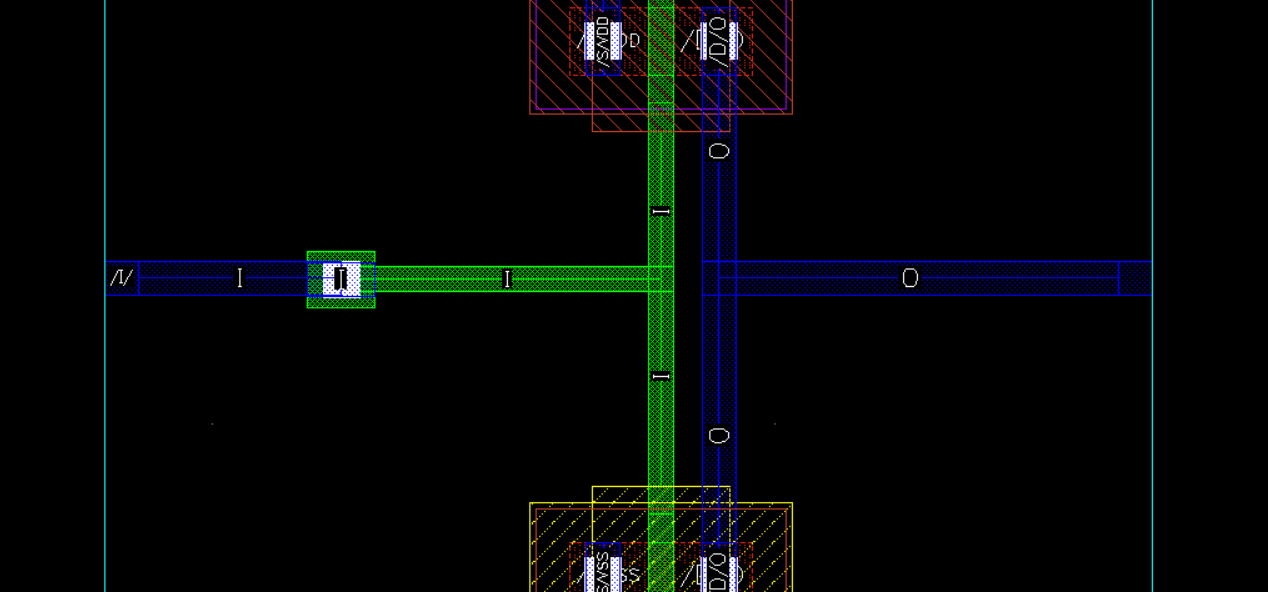
1. **OR GATE**

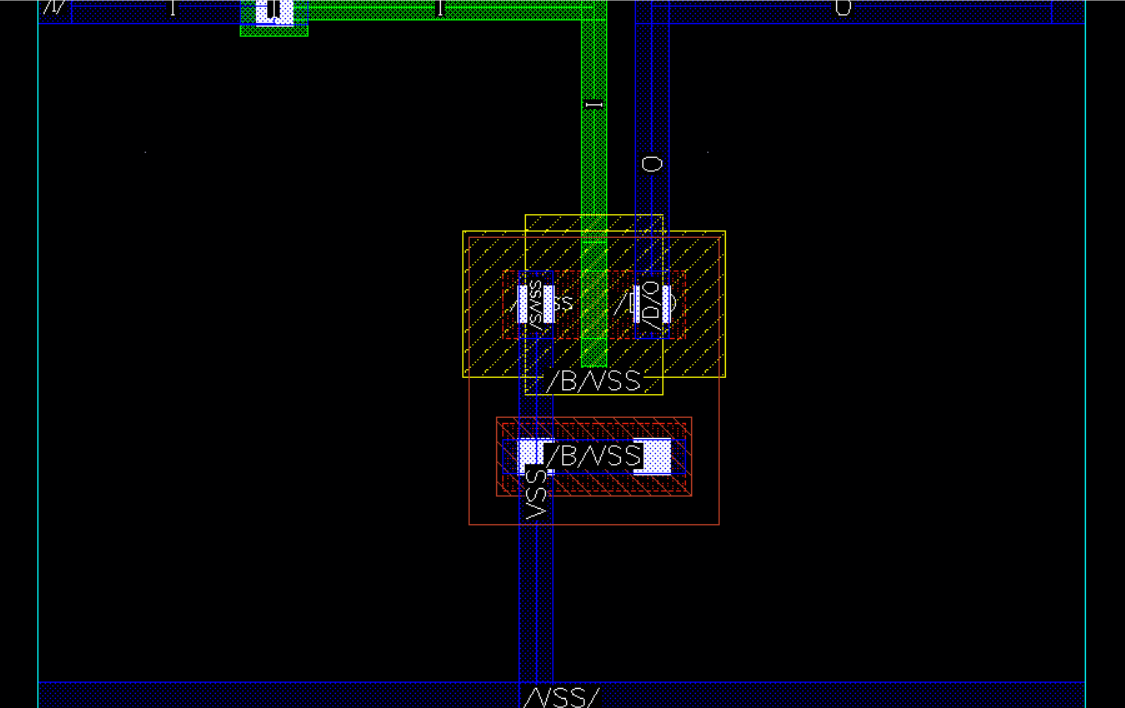
**1. Schemetic**

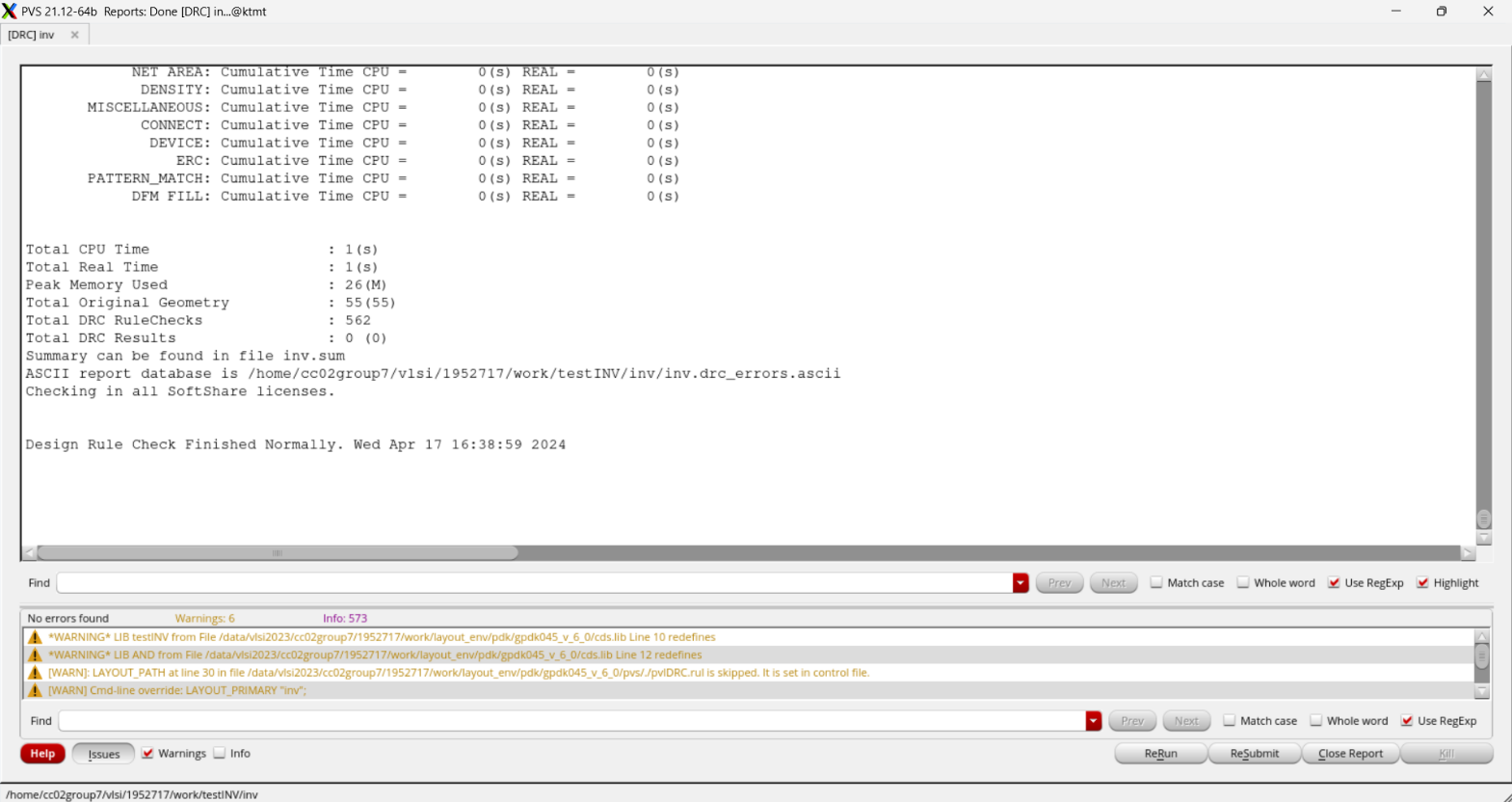
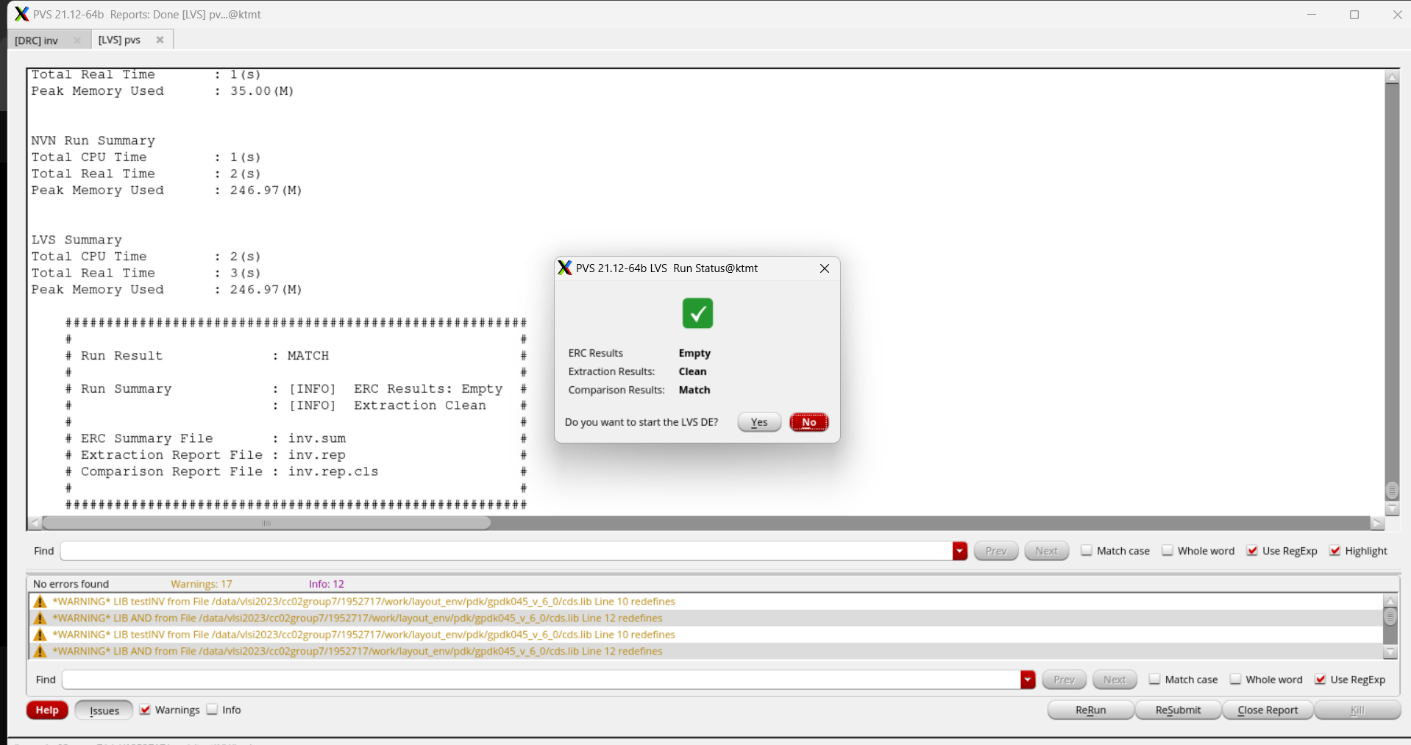
2. Simulation results

1. **Layout design of NOT Gate**







1. DRC Report
2. LVS Report